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# Wideband Harmonic Suppression of Grid-Connected Inverter With Small DC-Side Capacitance Under Weak Grids Considering the PLL Effect

Zuohang Hu, Xiangyang Xing, *Member, IEEE,* Yan Li, *Member, IEEE,* Haiyang Wang, Le Chang
Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—Grid-connected inverters with small dc-side capacitance offer cost advantages but suffer from a significant neutral-point (NP) voltage ripple, which introduces low-frequency harmonics into the grid current. Additionally, under weak grid conditions, background harmonics in the point of common coupling (PCC) voltage will also distort the grid current, especially when the phase-locked loop (PLL) is considered. Existing harmonic suppression methods struggle to simultaneously address current harmonics from two harmonic disturbance sources, and the influence of PLL is totally ignored. To address these issues, a harmonic impedance model considering the influence of PLL is derived, which reveals that the PLL provides a low-impedance path for the current harmonic introduced by the NP voltage ripple, while it causes amplification of the current harmonic introduced by the background harmonics. Thus, a novel impedance reshaping method based on impedance decoupling in the $dq$-frame is presented. The proposed method can adaptively reshape both the internal and external impedance of the inverter, enabling wideband suppression of current harmonics from multiple harmonic disturbance sources. Finally, experiments validate the proposed control method.**

***Index Terms*—Grid-connected inverter, small capacitance, harmonic suppression, PLL effect, weak grid.**

## I. Introduction

GRID-CONNECTED inverter is the key interface for power conversion between the renewable energy and the power grid, whose performance has a significant impact on the power quality [1], [2]. In practice, cost and efficiency are two important points for inverters, and therefore, usually a small capacitance three-level inverter with discontinuous pulse width modulation (DPWM) is an ideal solution to save cost and improve efficiency. Unfortunately, a large neutral-point (NP) voltage ripple will be introduced, resulting in grid current containing abundant low-frequency harmonics [3].

Moreover, Distributed Power Generation (DPG) systems are typically deployed in remote areas and thus are subject to long-distance transmission lines and weaker grid conditions [4], [5]. Under such grid conditions, the grid impedance cannot be ignored. Various nonlinear loads inject harmonic currents that flow through the grid impedance, resulting in the point of common coupling (PCC) voltage with significant low and medium frequency background harmonics [6]. These harmonics in the PCC voltage are further reflected in the grid current, leading to severe current distortion and degraded power quality [7], [8]. Therefore, grid current harmonics are introduced by both the background harmonics in the PCC voltage and the NP voltage ripple.

Under weak grid conditions, since the grid current is affected by the background harmonics in the PCC voltage, a series of PCC voltage compensation methods have been investigated. In [9] and [10], the PCC voltage is directly measured and fed forward to the output of the controller. To achieve more precise and effective harmonic suppression, the harmonic components of the PCC voltage or grid voltage are extracted, and those harmonic components are fed forward with an appropriate gain to suppress the grid current harmonics [11], [12], [13]. Actually, the essence of PCC voltage feedforward is an impedance reshaping strategy, which is equivalent to connecting a virtual impedance in parallel with the inverter output impedance [14], [15]. Therefore, based on the PCC voltage feedforward, a frequency-division virtual impedance reshaping strategy is proposed in [16], which improves the adaptability of the inverter to weak grids while maintaining sufficient suppression of PCC voltage harmonics simultaneously. However, the PCC voltage feedforward-based strategy mentioned above can only suppress the harmonics caused by background harmonics in the PCC voltage, while it is powerless against the harmonics caused by NP voltage ripple.

To suppress the harmonic components from two harmonic disturbance sources simultaneously, several direct current harmonic suppression methods have been investigated. The grid current harmonics can be mitigated by passive filters [17] or active power filters [18], but these methods inevitably introduce additional cost and power losses, and they may cause resonance problems. To achieve autonomous current harmonic suppression, several current controllers have been proposed such as resonant controllers [3], [19], [20] and repetitive controllers [21], [22]. In [3], the mechanism of harmonic generation due to the NP voltage ripple is analyzed in details, and a proportional integral resonant (PIR) controller with a notch filter are introduced to suppress the current harmonics. However, the PIR controller can only suppress harmonics at specific frequencies and cannot achieve wideband harmonic suppression. To increase the bandwidth of harmonic control, multiresonant controllers [19], [20] have been introduced, which employ multiple resonant modules to achieve high gain amplification and significant attenuation of the selected harmonics. In addition to multiresonant controller, repetitive controllers [21], [22] have also been applied for harmonic suppression due to their ability to eliminate periodic disturbances, including a wide range of low- and medium-frequency

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harmonics. However, the instability of these controllers under weak grid conditions remains a concern.

The instability issue under weak grid conditions is primarily caused by the interaction between the phase-locked loop (PLL) and the grid impedance. Some literature have studied the stability improvement of grid-connected inverter considering the PLL under weak grid conditions [23], [24], [25], [26]. Actually, the PLL also has a significant impact on harmonic suppression. In the low- and medium-frequency range, the negative impedance effect of the PLL leads to a significant decrease in the output impedance magnitude of the inverter, thereby affecting all harmonic disturbance sources in this frequency range. However, few studies in the existing literature have explored the impact of the PLL on low- and medium-frequency harmonics. In [27], the influence of PLL dynamics on the harmonic instability and harmonic amplification was considered for the first time, covering this gap. However, only the harmonic disturbances in the PCC voltage were considered, without accounting for other harmonic disturbance sources. In [28], two harmonic disturbance sources from distorted grids and nonlinear loads were considered for the virtual synchronous generator (VSG), and a hybrid harmonic suppression method was proposed. However, since no PLL is employed in the VSG, the adverse effects introduced by the PLL are not considered. In grid-connected inverter systems, the negative impedance introduced by the PLL couples the two harmonic disturbance sources, thereby creating conflicting impedance requirements for suppressing the harmonics contributed by each source.

Conventionally, according to reference frame in which the current and voltage signals are oriented, control schemes for grid-connected inverters can be broadly classified into synchronous $dq$-frame control and stationary $\alpha\beta$-frame control [3]. Regardless of control schemes, a PLL is required to synchronize with the grid for grid-following operation [29]. Therefore, the adverse impedance effect introduced by the PLL cannot be avoided independent of whether the controller is implemented in the $dq$-frame or the $\alpha\beta$-frame. Nevertheless, when PLL dynamics are considered, the two dominant harmonic disturbance sources can be naturally separated into different axes in the $dq$-frame, which makes impedance interpretation and decoupled controller design more straightforward. In fact, the coupling of the two harmonic disturbance sources introduced by the PLL is reflected in the coupling between the impedances of the $d$-axis and $q$-axis. To overcome these limitations, a harmonic impedance model considering the PLL is established, and an impedance-decoupling-based current harmonics suppression method is presented in the $dq$-frame. The contributions of this paper are summarized as follows.

1) A harmonic impedance model incorporating PLL dynamics is established to characterize harmonic behavior in grid-connected inverters, particularly in the low- and medium-frequency range under weak-grid conditions. Conventionally, only the impact of PLL on stability is considered, while its effect on harmonic is ignored.
2) With the impedance-based analysis, the impact of the PLL on two harmonic disturbances is revealed. Specifically, the PLL provides a low-impedance path for harmonics caused by NP voltage ripple, allowing these harmonics to flow into the inverter instead of the grid, while amplifying the current harmonics caused by background harmonics, which creating a conflict in impedance requirements and making the harmonic suppression more challenging.
3) An impedance reshaping method based on impedance decoupling in the $dq$-frame is proposed to resolve the conflicting impedance requirements introduced by the PLL. Both the internal and external impedance of the inverter are adaptively reshaped by this method, effectively mitigating current harmonics from multiple harmonic disturbance sources.

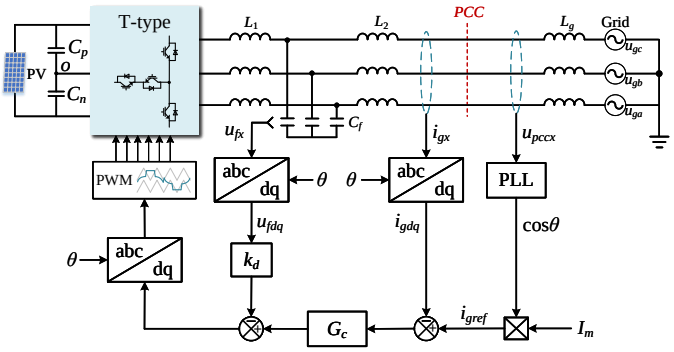


Fig. 1. General configuration and control scheme of a three-phase three-level T-type $LCL$-based inverter connected to grid.

The rest of this paper is organized as follows. The description of the inverter system and the harmonic impedance modeling are presented in Section II. Section III gives the requirements for virtual harmonic impedance the proposed impedance reshaping method. Section IV shows the experimental results. Finally, Section V concludes this paper.

## II. System Description and Harmonic Impedance Modeling

### A. System Configuration

Fig.1 shows the general configuration and control scheme of a three-phase grid-connected T-type inverter using an $LCL$ filter, where $L_1$, $L_2$ and $C_f$ are inverter-side inductors, grid-side inductors and filter capacitors, respectively. $L_g$ is the grid inductance, a pure inductor is considered to represent the worst-case stability scenario.To mitigate the $LCL$ resonance peak, an active damping coefficient $k_d$ for filter capacitor voltage feedback is introduced. $u_{pccabc}$ is PCC voltage, which is sensed by the PLL to obtain synchronous phase information and generate the grid current reference $i_{gref}$. A proportional integral (PI) controller $G_c$ is applied to achieve grid current tracking. In addition, to reduce switching losses and improve system efficiency, the discontinuous pulsewidth modulation (DPWM) strategy is commonly adopted.

$C_p$ and $C_n$ are the upper and lower dc-side capacitors. O is the NP of $C_p$ and $C_n$. The NP voltage $u_{np}$ at this point is defined as the voltage difference between the upper and lower

capacitors. The ripple of $u_{np}$ will significantly distort the grid current, which can be expressed as

$$u_{np} = u_p - u_n = \frac{\int \bar{I}_{np}\, d\omega t}{\omega C_{dc}} \tag{1}$$

where $u_p$ and $u_n$ are the upper and lower capacitor voltages, $\bar{I}_{np}$ is the average NP current, $\omega$ is the angular frequency, $C_{dc}$=$C_p$=$C_n$ is the capacitance of the dc-side capacitor.

It is seen from (1) that the NP voltage is affected by the dc-side capacitance. As the dc-side capacitance decreases, the NP voltage ripple increases. For cost-saving considerations, the dc-side capacitance is typically designed to be small, leading to pronounced NP voltage ripple, especially when DPWM strategy is employed.

### B. Analysis of Harmonic Challenge

Considering both the NP voltage ripple and background harmonics in the PCC voltage, taking phase A as an example, the reference voltage can be expressed as

$$\begin{aligned} u_{\mathrm{ref}\alpha} = {} & mU_{dc}\sin(\omega t) + 2u_{np}\frac{|mU_{dc}\sin(\omega t)|}{U_{dc}} \\ & + \sum_{n=5,7,11,\ldots} A_n \sin(n\omega t + \theta_n). \end{aligned} \tag{2}$$

where $m$ is the modulation index, $\theta_n$ is the phase angle of the $n$th harmonic, and $A_n$ is the magnitude of the $n$th background harmonics.

Based on (2) and the clamping characteristics of DPWM, the NP voltage $u_{np}$ fluctuates at three times the fundamental frequency. Therefore, the reference voltage can be rewritten as

$$\begin{aligned} u_{\mathrm{ref}\alpha} = {} & mU_{dc}\sin(\omega t) + 2mk_{np}\,\sin(3\omega t)\,|\sin(\omega t)| \\ & + \sum_{n=5,7,11,\ldots} A_n \sin(n\omega t + \theta_n). \end{aligned} \tag{3}$$

where $k_{np}$ is the peak value of the NP voltage ripple.

The disturbance term of the NP voltage ripple in (3) can be expressed using Fourier expansion as

$$\begin{aligned} u_{\mathrm{ref}\alpha} = {} & mU_{dc}\sin(\omega t) \\ & + \sum_{n=5,7,11,\ldots} \left[\, 2mk_{np}b_n \sin(n\omega t) + A_n \sin(n\omega t + \theta_n)\right]. \end{aligned} \tag{4}$$

where $b_n$ is the Fourier coefficient.

It is seen from (4) that the harmonic components caused by the large NP voltage ripple and background harmonics are mainly concentrated in the low- and medium-frequency range, such as the $5^{\mathrm{th}}$, $7^{\mathrm{th}}$, $11^{\mathrm{th}}$, $13^{\mathrm{th}}$, $17^{\mathrm{th}}$ and $19^{\mathrm{th}}$ harmonics. These harmonics will seriously distort the grid current and fail to meet the typical requirement of grid connection. Unfortunately, the impedance of the $LCL$ filter in this frequency band is low, reducing its ability to suppress the harmonic components caused by the large NP voltage ripple and background harmonics.

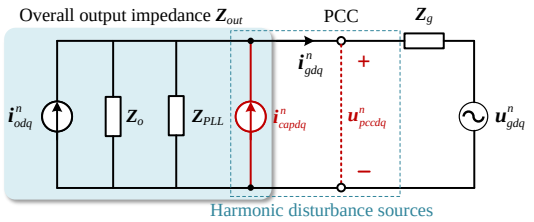


Fig. 2. Equivalent harmonic-domain circuits of the small dc-side capacitance grid-connected inverter.

### C. Harmonic Impedance Modeling

In addition to the well-known impact on the system stability, the PLL also plays a critical role in shaping the harmonic characteristics of the grid-connected inverter. The dynamic behavior of the PLL introduces a harmonic impedance component, which alters the overall harmonic impedance of the inverter, especially in the low- and medium-frequency range. The modified impedance reduces the ability to reject harmonics and may lead to the amplification of specific harmonics, which degrades the quality of the grid current.

To simplify the analysis, the coupling between the $d$-axis and $q$-axis is neglected since the decoupling control and the unity power factor operation are adopted [29]. Based on Fig. 1 and the Norton model, the equivalent harmonic-domain circuit of the grid-connected inverter with small capacitance considering the PLL dynamics is shown in Fig. 2. The equivalent harmonic impedance $\boldsymbol{Z}_{PLL}$ introduced by PLL dynamics is parallel to the inherent harmonic impedance of the inverter $\boldsymbol{Z}_o$. The harmonic disturbance caused by NP voltage ripple can be equivalent to a harmonic current source $\boldsymbol{i}^n_{capdq}$. In addition to the current harmonics introduced by NP voltage ripple, the PCC voltage usually contains abundant low- and medium-frequency background harmonics, which will also seriously distort the grid current and fail to meet the requirements of grid connection. Therefore, there are two harmonic disturbance sources in the system, and the resulting harmonics are wideband distributed. According to Fig. 2, the harmonic grid current $\boldsymbol{i}^n_{gdq}$ and harmonic PCC voltage $\boldsymbol{u}^n_{pccdq}$ can be expressed as

$$\begin{aligned} \boldsymbol{i}^n_{gdq} = {} & (\boldsymbol{Z}_{out} + \boldsymbol{Z}_g)^{-1}\boldsymbol{Z}_{out}\left(\boldsymbol{i}^n_{odq} + \boldsymbol{i}^n_{capdq}\right) \\ & - (\boldsymbol{Z}_{out} + \boldsymbol{Z}_g)^{-1}\boldsymbol{u}^n_{gdq} \end{aligned} \tag{5}$$

$$\boldsymbol{u}^n_{pccdq} = \boldsymbol{u}^n_{gqd} + \boldsymbol{i}^n_{gdq}\cdot\boldsymbol{Z}_g \tag{6}$$

where $\boldsymbol{i}^n_{odq}$ is Norton equivalent ideal harmonic current source of $n^{\mathrm{th}}$ harmonics, $\boldsymbol{Z}_{out}$ is the overall output harmonic impedance of the inverter.

Based on the control scheme in Fig. 1, the simplified grid current control block diagram considering the dynamics of PLL is shown in Fig. 3 [26]. By equivalent transformation, $G_{a1}$, $G_{a2}$ and the current loop gain $T_a$ is expressed as

$$\boldsymbol{G}_{a1} = \left[\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{Cf}\boldsymbol{k}_d\boldsymbol{K}_{\mathrm{pwm}}\boldsymbol{G}_d + \boldsymbol{Z}_{Cf}\right]^{-1}\boldsymbol{Z}_{Cf} \tag{7}$$

$$\begin{aligned} \boldsymbol{G}_{a2} = {} & [\boldsymbol{Z}_{L1}\boldsymbol{Z}_{L2} + \boldsymbol{Z}_{L2}\boldsymbol{Z}_{Cf}\boldsymbol{k}_d\boldsymbol{K}_{\mathrm{pwm}}\boldsymbol{G}_d + \boldsymbol{Z}_{Cf}\boldsymbol{Z}_T]^{-1} \\ & [\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{Cf}\boldsymbol{k}_d\boldsymbol{K}_{\mathrm{pwm}}\boldsymbol{G}_d + \boldsymbol{Z}_{Cf}] \end{aligned} \tag{8}$$

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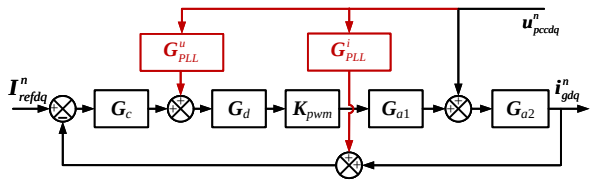


Fig. 3. Grid current control influenced by PLL.

$$\boldsymbol{T}_a = \boldsymbol{G}_c\boldsymbol{G}_d\boldsymbol{G}_{a1}\boldsymbol{G}_{a2} \tag{9}$$

where $\boldsymbol{Z}_{L1}$ , $\boldsymbol{Z}_{L2}$ and $\boldsymbol{Z}_{Cf}$ are the impedance of inverter-side inductor, grid-side inductor and filter capacitor, respectively. $\boldsymbol{Z}_T$ =$\boldsymbol{Z}_{L1}$+$\boldsymbol{Z}_{L2}$, $\boldsymbol{K}_{pwm}$ is the PWM gain, $\boldsymbol{G}_d$ represents the control delay.

The transfer matrices $\boldsymbol{G}^u_{PLL}$ and $\boldsymbol{G}^i_{PLL}$ related to the PLL dynamics are expressed as [25]

$$\boldsymbol{G}^i_{PLL} = \begin{bmatrix} 0 & 0 \\ 0 & -I_{gd0}H_{PLL} \end{bmatrix}. \tag{10}$$

$$\boldsymbol{G}^u_{PLL} = \begin{bmatrix} 0 & 0 \\ 0 & -U_{invd0}H_{PLL} \end{bmatrix}. \tag{11}$$

where $U_{invd0}$ and $I_{gd0}$ are the steady-state value of the inverter output voltage and grid current in the $d$-axis.

According to Fig. 3, the harmonic grid current $\boldsymbol{i}^n_{gdq}$ can be obtain as

$$\begin{aligned}\boldsymbol{i}^n_{gdq} = &\left[\boldsymbol{I}+\boldsymbol{T}_a\right]^{-1}\boldsymbol{T}_a\boldsymbol{I}^n_{refdq} - \left[\boldsymbol{I}+\boldsymbol{T}_a\right]^{-1}\boldsymbol{G}_{a2}\boldsymbol{u}^n_{pccdq} \\ &- \left[\boldsymbol{I}+\boldsymbol{T}_a\right]^{-1}\left[\boldsymbol{G}^i_{PLL}\boldsymbol{T}_a + \boldsymbol{G}^u_{PLL}\boldsymbol{G}_d\boldsymbol{G}_{a1}\boldsymbol{G}_{a2}\right]\boldsymbol{u}^n_{pccdq}\end{aligned} \tag{12}$$

where $\boldsymbol{I}$ is a $2\times 2$ identity matrix. According to the Norton equivalent, the harmonic grid current in (12) can be written as

$$\boldsymbol{i}^n_{gdq} = \boldsymbol{i}^n_{odq} - \left[\boldsymbol{Z}_o \parallel \boldsymbol{Z}_{PLL}\right]^{-1}\boldsymbol{u}^n_{pcdq} \tag{13}$$

It is seen from (13) that after considering PLL, the the overall output harmonic impedance of the inverter $\boldsymbol{Z}_{out}$ consists of two parts: $\boldsymbol{Z}_o$ and $\boldsymbol{Z}_{PLL}$. Accordingly, it can be expressed as

$$\boldsymbol{Z}_{out} = \boldsymbol{Z}_o \parallel \boldsymbol{Z}_{PLL} = \begin{bmatrix} Z_{outd} & 0 \\ 0 & Z_{outq} \end{bmatrix} \tag{14}$$

where $Z_{outd}$ and $Z_{outq}$ are the overall output harmonic impedance of $d$-axis and $q$-axis. Substituting (10)-(13) into (14), $Z_{outd}$ and $Z_{outq}$ can be expressed as

$$Z_{outd} = Z_o = \frac{1+T_a}{G_{a2}} \tag{15}$$

$$\begin{aligned}Z_{outq} &= Z_o \parallel Z_{PLL} \\ &= \frac{1+T_a}{G_{a2} + U_{invd0}H_{PLL}T_a + I_{gd0}H_{PLL}G_dG_{a1}G_{a2}}\end{aligned} \tag{16}$$

where $H_{PLL}$ is the transfer function of the PLL, which can be obtained by the small-signal model of PLL dynamics [27].

It is clearly seen from (15) and (16) that after considering the PLL, the output harmonic impedance of the $d$-axis remains unaffected. The PLL dynamics affect only the output harmonic impedance of the $q$-axis. In addition, it should be noted that the above conclusion is valid under the assumption that the coupling of the $dq$-axis is ignored and unity power factor operation is adopted. If the $dq$-axis decoupling and unity power factor operation are not adopted, the harmonic impedance variation introduced by the PLL would be mixed with the cross-coupling between the $d$- and $q$-axes, making it much more difficult to clearly reveal the dominant mechanism that the PLL mainly affects the $q$-axis harmonic impedance. Nevertheless, removing this assumptions cannot invalidate the main PLL-induced mechanism revealed in this paper, but it only makes the model more strongly coupled and the corresponding analytical results less clear.

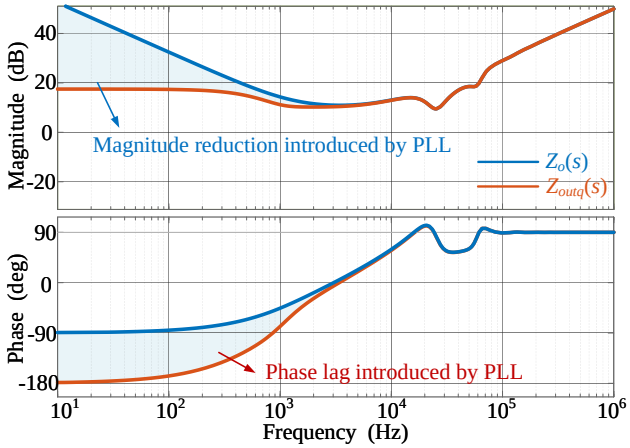


Fig. 4. Bode diagram of the output harmonic impedance considering the PLL effect.

TABLE I
EXPERIMENTAL PARAMETERS.

| Parameters | Value |
|---|---|
| Grid voltage ($U_g$) | 110 Vres |
| DC-side voltage ($U_{dc}$) | 350 V |
| DC-side capacitance ($C_p$ and $C_n$) | 220 $\mu$F |
| Inverter-side inductance ($L_1$) | 1 mH |
| Grid-side inductance ($L_2$) | 0.5 mH |
| Filter capacitance ($C_f$) | 4.7 $\mu$F |
| Grid impedance ($L_g$) | 2.5 mH, 8 mH |
| Switching frequency ($f_{sw}$) | 5 kHz |
| Sampling frequency ($f_s$) | 10 kHz |
| PLL parameter ($k_{ppll}$ and $k_{ipll}$) | 6.1 2636.3 |

Fig. 4 shows the Bode diagram of $Z_o$ and $Z_{outq}$, where the parameters are listed in Table I. It is seen that the introduction of PLL reduces the magnitude of the equivalent output harmonic impedance in the low- and medium-frequency band. Therefore, in the $q$-axis, the harmonics from the voltage disturbance source $u^n_{pccq}$ are amplified due to the reduction of the output harmonic impedance, while those from the current disturbance source $i^n_{capq}$ are attenuated since the majority of the harmonic components flow into the inverter instead of the grid. In the $d$-axis, since the output harmonic impedance is not affected by the PLL and remains relatively high, its effect on the two harmonic disturbance sources is opposite to that in the $q$-axis.

To more clearly investigate the distinct effects of the two harmonic disturbance sources on the $d$-axis and $q$-axis current harmonic components, Fig. 5 shows the relationships between$i^n_{gd}$, $i^n_{capd}$, $Z_{outd}$, $i^n_{gq}$, $u^n_{gq}$ and $Z_{outq}$ according to (5) and (6). As shown in Fig. 5(a), in the $d$-axis, $i^n_{gd}$ is positively correlated with $i^n_{capd}$ and $Z_{outd}$. With the increase of $Z_{outd}$,

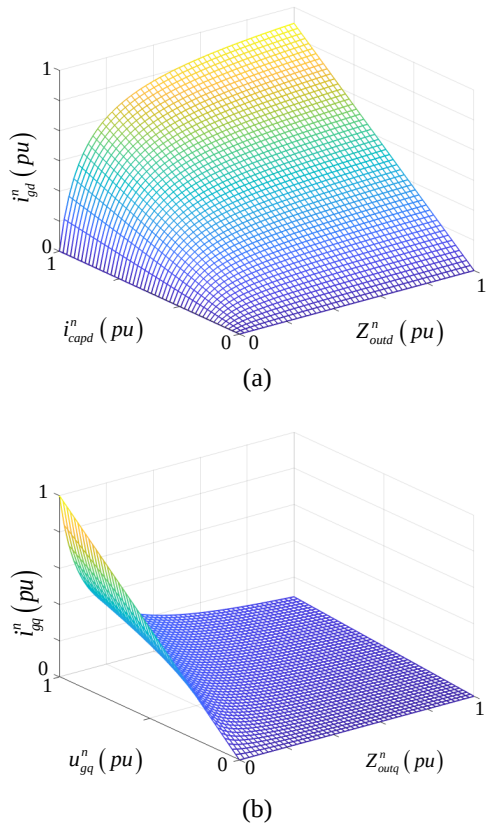


Fig. 5. Relationships of the grid current harmonics in the $dq$-axis. (a) Relationship between $i^n_{gd}$, $i^n_{capd}$ and $Z_{outd}$ in $d$-axis. (b) Relationship between $i^n_{gq}$, $u^n_{gq}$ and $Z_{outq}$ in $q$-axis.

a large portion of $i^n_{capd}$ is injected into the grid instead of the inverter, leading to an increase in grid current harmonics. In this case, there are two ways to reduce $i^n_{gd}$: decrease $i^n_{capd}$ or lower $Z_{outd}$. In the $q$-axis, the PLL effect reduces the equivalent impedance of the PCC to the inverter, so that most of the harmonic disturbance introduced by $i^n_{capd}$ flows into the inverter instead of the grid, accordingly, the harmonic disturbance from NP voltage ripple can be neglected. As $Z_{outq}$ decreases, the damping effect of the current loop impedance on the background harmonics in $u^n_{gq}$ is weakened, resulting in an increase of harmonics in grid current. Therefore, $i^n_{gq}$ is positively correlated with $u^n_{gq}$ but negatively correlated with $Z_{outq}$ as shown in Fig. 5(b). There are also two ways to reduce $i^n_{gq}$: decrease $u^n_{gq}$ or increase $Z_{outq}$. The disturbance sources $i^n_{capd}$ and $u^n_{gq}$ are determined by external factors of the system cannot be easily adjusted. Therefore, to reduce the current harmonic components, it is necessary to decrease $Z_{outd}$ and increase $Z_{outq}$. Consequently, there exists a conflict in the $dq$-axis at the two harmonic disturbance sources.

Fortunately, this conflict can be resolved through the impedance decoupling in the $dq$-frame. Since the PLL only affects the $q$-axis, the dominant harmonic disturbances originate from $i^n_{capd}$ in the $d$-axis and from $u^n_{pccq}$ in the $q$-axis. To effectively mitigate the harmonic from the two disturbance sources, different virtual impedances need to be introduced on the $d$-axis and $q$-axis, which ensures more precise control over the harmonic sources originating from $i^n_{capd}$ and $u^n_{pccq}$.

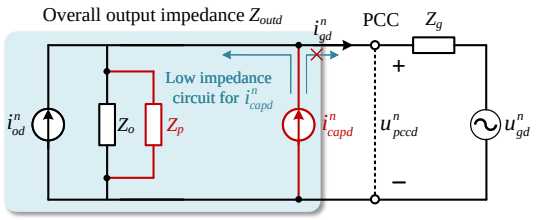


Fig. 6. Equivalent harmonic impedance circuit of the proposed method in $d$-axis.

## III. Proposed Impedance-Based Grid Current Harmonic Suppression Scheme

### A. Impedance Decoupling in the $dq$-Frame

Since variations in the inverter output harmonic impedance impose opposite effects on the harmonics originating from the two disturbance sources, their impedance requirements are inherently coupled. Consequently, harmonic suppression cannot be effectively achieved by merely adjusting the overall inverter output impedance. To address this limitation, an impedance decoupling approach in the $dq$-frame is proposed, in which the harmonic impedances in the $d$- and $q$-axis are independently designed to decouple their requirements and suppress different harmonic disturbance sources.

In the $d$-axis, the relative high output harmonic impedance provides strong damping of the harmonics in the PCC voltage. Therefore, the harmonic disturbance source $u^n_{pccd}$ is negligible as shown in Fig. 6. For the harmonic disturbance source $i^n_{capd}$, the harmonic current can either flow into the inverter side with an impedance of $Z_{outd}$ or into the grid side with an impedance of $Z_g$. To suppress the harmonic components flowing into the grid side, the impedance of the alternative harmonic current path, i.e., the inverter impedance $Z_{outd}$, needs to be reduced. Therefore, a virtual impedance $Z_p$ is introduced in parallel with the inverter output impedance, forming a parallel virtual impedance branch as shown in Fig. 6. This branch is designed to exhibit much lower impedance at harmonic frequencies compared to both the inverter output impedance and the grid impedance, thereby guiding most of the harmonic current into this low-impedance path instead of the grid. Then, the grid current harmonic component in the $d$-axis is derived as

$$i^n_{gd} = \frac{Z_{outd-p}}{Z_{outd-p} + Z_g}\left(i^n_{od} + i^n_{capd}\right) \tag{17}$$

where $Z_{outd-p}$ is the overall inverter output impedance in $d$-axis after introducing $Z_p$, which is expressed as

$$Z_{outd-p} = Z_o \parallel Z_p \tag{18}$$

In the $q$-axis, the equivalent harmonic impedance $Z_{PLL}$ introduced by the PLL is paralleled with the inherent output harmonic impedance $Z_o$, resulting in a decreased magnitude of the overall inverter output impedance. Therefore, most of the harmonics from $i^n_{capq}$ flows into the inverter and the dominate harmonic disturbance source is the $u^n_{pccq}$ as shown in Fig. 7. It is seen that the introduction of the PLL significantly reduces the impedance of the background harmonic loop, amplifying the grid current harmonics, which is one of the main reasons

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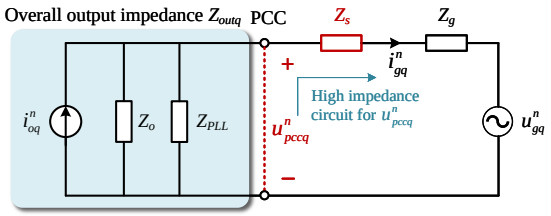


Fig. 7. Equivalent harmonic impedance circuit of the proposed method in $q$-axis.

for the enhancement of harmonic coupling. To address this issue, a virtual impedance $Z_s$ is incorporated in series with the overall output harmonic impedance $Z_{outq}$ in the grid-side branch to increase the impedance magnitude at background harmonic frequencies and fulfill the impedance requirements for an effective harmonic suppression as shown in Fig. 6. Based on Fig. 7, the harmonic grid current can be expressed as

$$i^n_{gq} = \frac{Z_o \parallel Z_{PLL}}{Z_{outq-s} + Z_g} i^n_{oq} - \frac{1}{Z_{outq-s}} u^n_{pccq} \tag{19}$$

where $Z_{outq-s}$ is the overall inverter output impedance in $q$-axis after introducing $Z_s$, which is expressed as

$$Z_{outq-s} = Z_o \parallel Z_{PLL} + Z_s \tag{20}$$

In addition to harmonic issues in the $q$-axis, the introduction of PLL shapes the inverter output impedance into a negative resistance as shown in Fig. 4, which is responsible for instability. Therefore, the design of $Z_s$ should comprehensively account for both harmonic suppression and stability improvement.

### *B. Proposed Wideband Harmonic Suppression Method*

According to Figs. 6 and 7, the impedance-based harmonic suppression control block diagram in the $dq$-frame is shown in Fig. 8. As indicated by the dashed line in Fig. 8, the series and parallel virtual impedances are introduced into the system. The introduction of $\boldsymbol{Z}_p$ in the PCC voltage feedforward loop is equivalent to a parallel virtual impedance, which is used to suppress the current harmonics in the $d$-axis caused by the NP voltage ripple. Meanwhile, the introduction of $\boldsymbol{Z}_s$ in the grid current feedback loop acts as a series virtual impedance, which serves to attenuate the current harmonics in the $q$-axis resulting from the background harmonics. The closed-loop transfer function of the system can be expressed in the Norton equivalent form as follows

$$\boldsymbol{i}^n_{gdq} = \boldsymbol{G}_{dq}\, \boldsymbol{I}^n_{refdq} - \boldsymbol{Z}^{-1}_{dq} \boldsymbol{u}^n_{pccdq} \tag{21}$$

where $\boldsymbol{G}_{dq}$ is the coefficient of the Norton equivalent current source, $\boldsymbol{Z}_{dq}$ is the equivalent harmonic impedance, which can be expressed as

$$\begin{aligned}\boldsymbol{G}_{dq} = \Big[ & \boldsymbol{Z}_p\big(\boldsymbol{Z}_{L1}\boldsymbol{Z}_{L2} + \boldsymbol{Z}_{Cf}(\boldsymbol{G}_c\boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}} \\ & + \boldsymbol{Z}_{L1} + \boldsymbol{Z}_{L2})\big) + \boldsymbol{Z}_s(\boldsymbol{Z}_{L1}\boldsymbol{Z}_{Cf}) \\ & + (\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{Cf})(\boldsymbol{Z}_{L2} + \boldsymbol{Z}_p)\Big]^{-1} \boldsymbol{G}_c\boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}}\boldsymbol{Z}_{Cf}\boldsymbol{Z}_p\end{aligned} \tag{22}$$

$$\begin{aligned}\boldsymbol{Z}_{dq} = & \Big[\, \boldsymbol{Z}_{L1}\boldsymbol{Z}_{Cf} + (\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{Cf})(\boldsymbol{Z}_{L2} + \boldsymbol{Z}_p)\,\Big]^{-1} \\ & \Big[\, \boldsymbol{Z}_p(\boldsymbol{Z}_{L1}\boldsymbol{Z}_{L2} + \boldsymbol{Z}_{Cf}(\boldsymbol{G}_c\boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}} + \boldsymbol{Z}_{L1} + \boldsymbol{Z}_{L2})) \\ & + \boldsymbol{Z}_s(\boldsymbol{Z}_{L1}\boldsymbol{Z}_{Cf} + (\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{Cf})(\boldsymbol{Z}_{L2} + \boldsymbol{Z}_p))\Big]\end{aligned} \tag{23}$$

where $\boldsymbol{Z}_p$ and $\boldsymbol{Z}_s$ is the second-order matrix of $Z_p$ and $Z_s$, which are expressed as

$$\boldsymbol{Z}_p = \begin{bmatrix} Z_p & 0 \\ 0 & 0 \end{bmatrix}, \quad \boldsymbol{Z}_s = \begin{bmatrix} 0 & 0 \\ 0 & Z_s \end{bmatrix} \tag{24}$$

To simplify the implementation, an equivalent transformation is applied to the series and parallel virtual impedances. Following the transformation, the series virtual impedance is embedded in the grid-current feedback loop with a gain of $\boldsymbol{H}_s$, while the parallel virtual impedance is incorporated into the PCC voltage feedforward loop with a gain of $\boldsymbol{H}_p$. Based on Fig. 8, after the equivalent transformation, the system remains in the Norton equivalent form as shown in (21), where the coefficient of the Norton equivalent current source and equivalent impedance are expressed as

$$\begin{aligned}\boldsymbol{G}_{eqdq} = & \Big[\, (\boldsymbol{I} + \boldsymbol{H}_s)\,\boldsymbol{G}_c\boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}}\boldsymbol{Z}_{Cf} + \boldsymbol{Z}_{Cf}(\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{L2}) \\ & + \boldsymbol{Z}_{L1}\boldsymbol{Z}_{L2}\,\Big]^{-1} \boldsymbol{G}_c\boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}}\boldsymbol{Z}_{Cf}\end{aligned} \tag{25}$$

$$\begin{aligned}\boldsymbol{Z}_{eqdq} = & \Big(\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{Cf} + \boldsymbol{H}_p\boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}}\boldsymbol{Z}_{Cf}\Big)^{-1} \Big[(\boldsymbol{I} + \boldsymbol{H}_s) \\ & \boldsymbol{G}_c\boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}}\boldsymbol{Z}_{Cf} + \boldsymbol{Z}_{Cf}(\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{L2}) + \boldsymbol{Z}_{L1}\boldsymbol{Z}_{L2}\Big]\end{aligned} \tag{26}$$

To achieve the same effect before and after equivalent transformation, the coefficient of the Norton equivalent current source and equivalent impedance in (22) and (23) should be equal to their corresponding counterparts in (25) and (26), which are expressed as

$$\begin{cases} \boldsymbol{G}_{dq} = \boldsymbol{G}_{eqdq} \\ \boldsymbol{Z}_{dq} = \boldsymbol{Z}_{eqdq} \end{cases} \tag{27}$$

By solving (27), the feedforward gain of the PCC voltage $\boldsymbol{H}_p$ and feedback gain of the grid current $\boldsymbol{H}_s$ are expressed as

$$\boldsymbol{H}_p = \Big[\, \boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}}\boldsymbol{Z}_{Cf}\boldsymbol{Z}_p \,\Big]^{-1} \Big[\, \boldsymbol{Z}_{L1}\boldsymbol{Z}_{Cf} + \boldsymbol{Z}_{L2}\big(\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{Cf}\big) \,\Big] \tag{28}$$

$$\begin{aligned}\boldsymbol{H}_s = & \Big[\, \boldsymbol{G}_c\boldsymbol{G}_d\boldsymbol{K}_{\text{pwm}}\boldsymbol{Z}_{Cf}\boldsymbol{Z}_p \,\Big]^{-1} \\ & \Big[\, \boldsymbol{Z}_s\Big((\boldsymbol{Z}_{L1} + \boldsymbol{Z}_{Cf})(\boldsymbol{Z}_{L2} + \boldsymbol{Z}_p) + \boldsymbol{Z}_{L1}\boldsymbol{Z}_{Cf}\Big) \,\Big]\end{aligned} \tag{29}$$

For the parallel virtual impedance $Z_p$, the design objective is to minimize its magnitude at harmonic frequencies to reduce the impedance of the harmonic disturbance source $i^n_{capd}$ loop. While at other frequencies, the magnitude of $Z_p$ should remain sufficiently high to enhance the damping characteristics of the grid current loop against low- and medium- frequency harmonics. Thus, $Z_p$ can be implemented as a notch filter with a proportional gain $K_{pp}$, which is expressed as

$$Z_p = K_{pp} \cdot \frac{s^2 + \omega^2_{r1}}{s^2 + s\omega_{r1}/Q + \omega^2_{r1}} \tag{30}$$

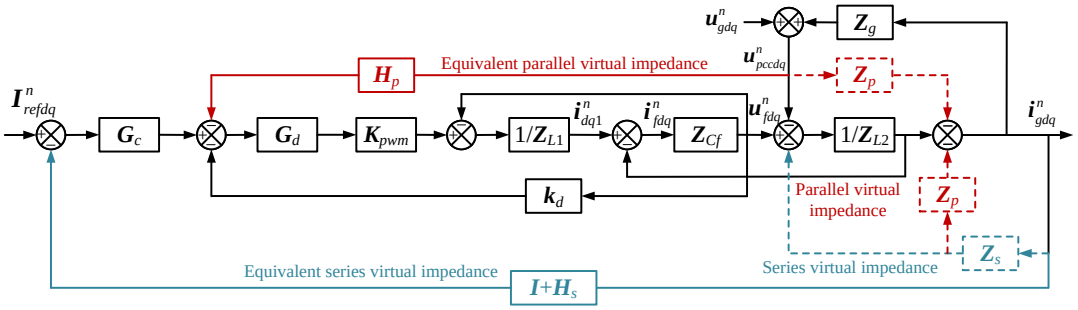


Fig. 8. Equivalent control block diagram of the wideband harmonic suppression method.

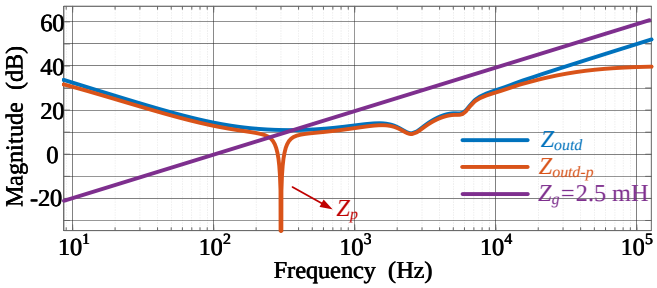


Fig. 9. Bode diagram of the parallel virtual impedance included in Fig. 6.

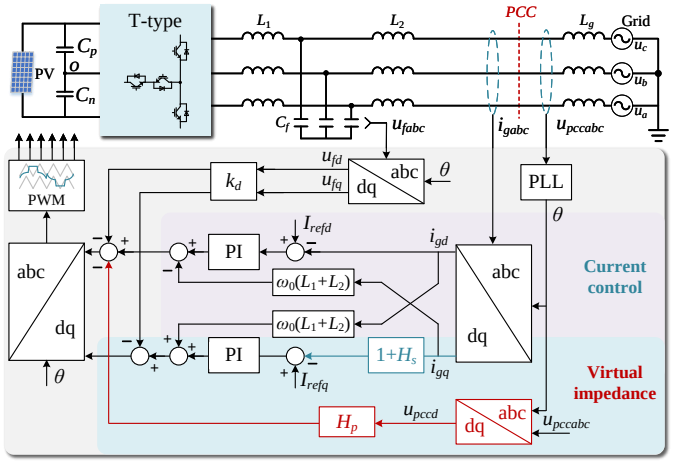


Fig. 10. Overall control block diagram of the proposed method.

where $Q$ is the quality factor, $\omega_{r1}$ is the central angular frequency of the notch filter. Since the harmonics components in $i^n_{capd}$ caused by the NP voltage ripple are mainly the $5^{\text{th}}$ and $7^{\text{th}}$ harmonics, which are characterized as $6^{\text{th}}$ harmonic in the $dq$-frame. Therefore, $\omega_{r1}$ is selected as 6 times the fundamental angular frequency.

After introducing the parallel virtual impedance $Z_p$, the magnitude-frequency response curve of the overall output harmonic impedance in the $d$-axis is shown in Fig. 9. With the integration of the parallel virtual impedance $Z_p$, the harmonic impedance of $Z_{outd-p}$ is effectively restricted and remains lower than the grid impedance $Z_g$ at the targeted harmonic frequencies. Consequently, the harmonic components in $i^n_{capd}$ predominantly flow into the inverter, minimizing their injection into the grid. Moreover, due to the presence of the proportional gain $K_{pp}$, $Z_{outd-p}$ exhibits minimal attenuation at other harmonic frequencies compared to $Z_{outd}$, which retains the harmonic rejection performance of the grid current loop.

The design objective of the series virtual impedance $Z_s$ is to maximize the magnitude at the frequencies of background harmonics in $u^n_{pccq}$, thus enhancing the harmonic damping effect at these frequencies. Therefore, a multi-resonant controller is introduced in $Z_s$. In addition, system instability issue should also be addressed in the $q$-axis due to the negative resistance characteristics introduced by the PLL. Fortunately, the instability can be successfully mitigated by adopting a virtual series-based positive resistance [30]. Considering both harmonic suppression and system stability, the series virtual impedance $Z_s$ can be designed as a multi-resonant controller with the proportional link, which is expressed as

$$Z_s = K_{ps} + \sum_{n=6,12,18} \frac{2K_{rn}\,\omega_{cn}\,s}{s^2 + 2\omega_{cn}s + (n\omega_0)^2} \tag{31}$$

where $K_{rn}$ is the gain of resonant controller, $\omega_0$ is the fundamental angular frequency of the resonant controller, $\omega_{cn}$ is the bandwidth factor. $K_{ps}$ is the proportional link, which is equivalent to a virtual positive resistance in $Z_s$.

After the parallel virtual impedance $Z_p$ and the series virtual impedance $Z_s$ are determined, the overall control block diagram of the proposed method is shown in Fig. 10, which includes the PLL, the capacitor voltage feedback loop, the $dq$-frame current control loop and the two virtual impedance branches. Specifically, the parallel virtual impedance $Z_p$ is designed in the $d$-axis and introduced through the PCC voltage feedforward path to suppress the current harmonics caused by the NP voltage ripple, while the series virtual impedance $Z_s$ is designed in the $q$-axis and introduced through the grid current feedback path to attenuate the current harmonics induced by background harmonics in the PCC voltage and simultaneously improve weak grid stability.

Fig. 11 shows the Bode diagram of the overall output harmonic impedance in the $q$-axis. By increasing the impedance magnitude of $Z_{outq}$ at the major harmonic frequencies through the series virtual impedance $Z_s$, the adverse effects of impedance magnitude reduction caused by the PLL is

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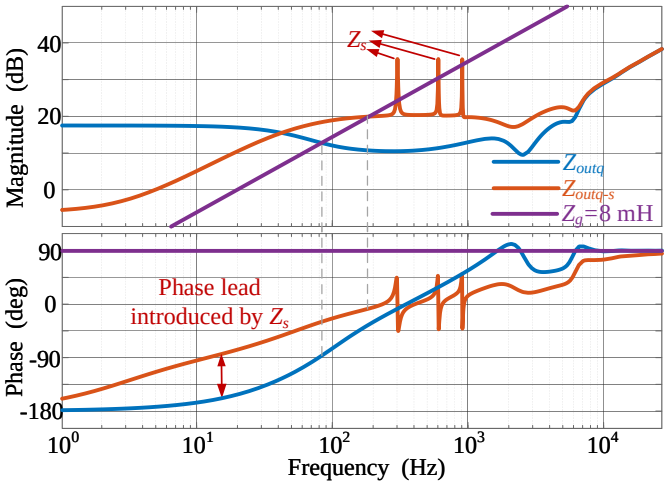


Fig. 11. Bode diagram of the series virtual impedance included in Fig. 7.

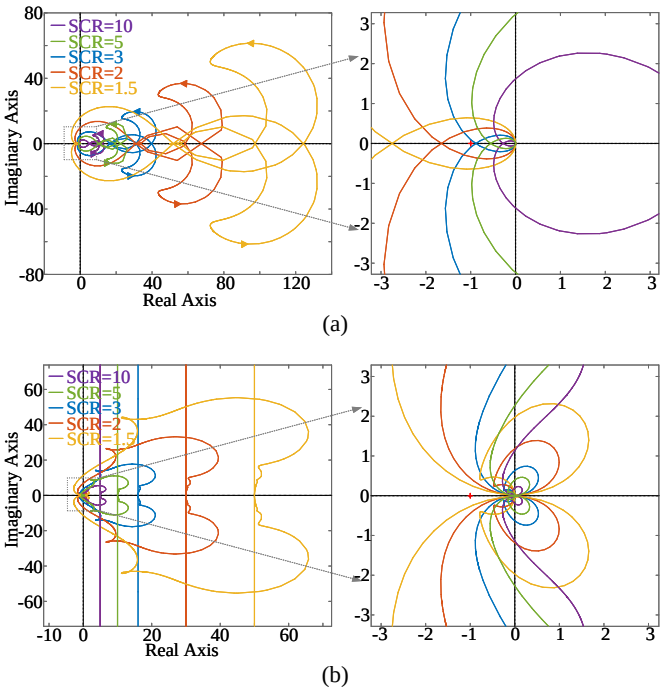


Fig. 12. Nyquist plots of impedance ratio with different grid strengths. (a) $Z_g/Z_{outq}$. (b) $Z_g/(Z_{outq}+Z_s)$.

mitigated. Therefore, the background harmonics can be effectively suppressed, achieving wideband harmonic suppression. Furthermore, since the proportional link in (31) is equivalent to a series virtual positive resistance, the phase characteristics in the low- and medium- frequency range are significantly improved, the negative resistance effect introduced by the PLL is eliminated. Therefore, based on the Nyquist stability criterion, incorporating $Z_s$ leads to a substantial enhancement of the system stability margin as illustrated in Fig. 11.

To further demonstrate how $Z_s$ mitigates the negative resistance effect introduced by the PLL, Fig. 12 presents the Nyquist plots of the impedance ratio $Z_g/Z_{outq}$ and $Z_g/(Z_{outq}+Z_s)$ with different grid strengths. It is seen from Fig. 12(a) that when SCR $<$ 3, the root loci encircle the point (-1, j0) and the system becomes unstable. Nevertheless, after introducing $Z_s$, none of the root loci encircle the point (-1, j0) as shown in Fig. 12(b), which indicates that the proposed method exhibits strong robustness against grid impedance variation. Even when the grid impedance increases and the grid becomes weaker, the introduction of $Z_s$ can still effectively suppress the PLL-induced negative resistance effect and maintain stable operation over a wide range of grid strengths.

### C. Design of the Virtual Impedance $Z_p$ and $Z_s$

The parallel virtual impedance $Z_p$ is used to divert the grid current harmonic components caused by the NP voltage ripple into the inverter instead of the grid. To ensure sufficient robustness of $Z_p$, its design should consider the impact of grid frequency fluctuations. It is mentioned in [31] that the allowable fluctuation range of the grid frequency is ±0.5 Hz. Thus, the frequency fluctuation range at the $6^{\text{th}}$ harmonic is ±3 Hz and the control bandwidth is 6 Hz. In the notch filter, the relationship between the quality factor $Q$ and the control bandwidth $B$ can be expressed as [3]

$$Q = \sqrt{\frac{\omega_{r1}^2 + \omega_{r1}\sqrt{\omega_{r1}^2 + B^2}}{2B^2}} \tag{32}$$

Therefore, the quality factor $Q$ can be determined according to (32). After introducing the parallel virtual impedance $Z_p$, the magnitude of the inverter output impedance in the $d$-axis decreases at high frequencies, which weakens the attenuation of high-frequency harmonic components. Therefore, the purpose of introducing the proportional gain $K_{pp}$ in $Z_p$ is to keep the magnitude of $Z_p$ sufficiently high and increase the overall inverter output impedance, thereby enhancing the damping characteristics of the grid current loop against high-frequency harmonics. In this paper, the design ensures that at the switching frequency $f_{sw}$, the reduction of the overall inverter output impedance in the $d$-axis after introducing $Z_p$ is kept within 10%, which can be expressed as

$$1 - \left| \frac{Z_{outd}(j2\pi f_{sw}) \parallel Z_p(j2\pi f_{sw})}{Z_{outd}(j2\pi f_{sw})} \right| < 10\% \tag{33}$$

Thus, (33) can be the condition for determining the value of $K_{pp}$.

The series virtual impedance $Z_s$ is used to suppress grid current harmonics induced by background harmonics in the grid voltage and to enhance stability under weak grid conditions. In (31), $\omega_{cn}$ is the bandwidth coefficient of the resonant controller at each resonant frequency, which can also be selected according to the grid-frequency fluctuation standard of ±0.5 Hz.

Since the proportional link $K_{ps}$ is mainly used to enhance system stability, its effect can be neglected when designing the resonance gain $K_{rn}$. In this case, the series virtual impedance can be expressed as

$$Z_{s,res} = \sum_{n=6,12,18} \frac{2K_{rn}\omega_{cn}s}{s^2 + 2\omega_{cn}s + (n\omega_0)^2} \tag{34}$$

To suppress the current harmonics introduced by the background harmonics, the magnitude of the overall inverter output impedance in the $q$-axis should not be overly small. Therefore, the minimum magnitude of the output impedance at each harmonic frequency should satisfy [32]

$$|Z_{outq}(j2\pi f_n) + Z_{s,res}(j2\pi f_n)| \geq \frac{U_g U_n}{I_g I_n} \tag{35}$$

where $f_n$ is the harmonic frequency, $U_g$ and $I_g$ are the root mean square (RMS) of the grid voltage and current, respectively. $U_n$ and $I_n$ are the distorted restriction ratio of the grid voltage and current, respectively. Therefore, according to (35), the allowable range of the resonance gain $K_{rn}$ can be determined.

The proportional link $K_{ps}$ is equivalent to the virtual positive resistance in $Z_s$, which is used to compensate for the negative resistance introduced by the PLL. To increase the stability margin, the inverter output impedance magnitude at intersection frequency $f_{sec}$, where the inverter output impedance intersects the grid impedance, should be greater than that without $K_{ps}$. In addition, to ensure system stability in the worst case, e.g., SCR=1.5, a large phase margin should be retained in practical applications [30], accordingly

$$|Z_{outq}(j2\pi f_{sec}) + K_{ps}| \geq |Z_{outq}(j2\pi f_{sec})| \tag{36}$$

$$\angle(Z_{outq}(j2\pi f_{sec}) + K_{ps}) \geq -(90 - \alpha)^\circ \tag{37}$$

where $\alpha$ is the desired phase margin.

In addition to the stability margin requirement, the design of $K_{ps}$ should also satisfy the steady-state error requirement. Excessive $K_{ps}$ will increase the grid current steady error compared with that without $K_{ps}$. Defining the steady-error of the grid current introduced by $K_{ps}$ as follows [30]

$$E_i = \left| \frac{i'_g(j\omega_0) - i_g(j\omega_0)}{i_g(j\omega_0)} \right| = \left| \frac{K_{ps}}{Z_{outq}(j\omega_0) + Z_g(j\omega_0) + K_{ps}} \right| \tag{38}$$

where $i'_g$ and $i_g$ are the grid current with and without the series virtual impedance, respectively. Therefore, the value of $K_{ps}$ can be determined according to (36)-(38).

According to the above design process of $Z_p$ and $Z_s$, their design is primarily determined by the targeted harmonic frequencies and the required impedance shaping characteristics. Therefore, parameter variations of the $LCL$ filter do not change the design objective or the fundamental mechanism of the proposed virtual impedances. However, variations in $L_1$, $L_2$ and $C_f$ may affect the practical implementation of $Z_p$ and $Z_s$ through the transfer functions $H_p$ and $H_s$ defined in (28) and (29). In other words, parameter mismatch may modify the quantitative impedance-reshaping result, such as the effective gain or phase characteristics realized by the virtual impedances. Nevertheless, such mismatch does not alter the fundamental mechanism of the proposed method or significantly weaken its harmonic suppression capability, indicating that the proposed method remains sufficiently robust against the parameter variations.

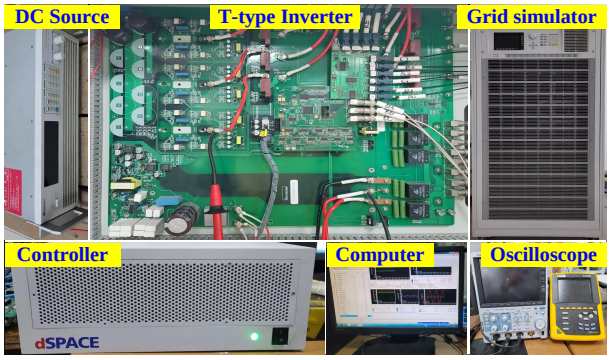


Fig. 13. Prototype of the small capacitance value grid-connected inverter.

## IV. Experimental Results

To verify the effectiveness of the proposed method, a three-phase T-type inverter prototype with $LCL$ filter has been constructed as shown in Fig. 13. The experimental parameters are listed in Table I. The dc-side capacitance is set to 220 $\mu$F to simulate the small capacitance value condition.

In the experiments, four methods are compared, which are summarized in Table II. Method-I is without harmonic suppression strategy (i.e., the conventional dual-loop current control with PI controller in the $dq$-frame) as shown in Fig. 14(a). Method-II uses the multi-resonant controller in the $\alpha\beta$-frame within the current control loop [19], [20] as shown in Fig. 14(b). Specifically, a proportional-resonant (PR) controller $\boldsymbol{G}_{PR}$ is adopted to track the fundamental component of the current reference, ensuring proper synchronization with the grid. Additionally, a multi-resonant controller $\boldsymbol{G}_{MR}$ are introduced at specific harmonic frequencies such as $5^{\text{th}}$, $7^{\text{th}}$, $11^{\text{th}}$, $13^{\text{th}}$, $17^{\text{th}}$ and $19^{\text{th}}$ to effectively suppress the harmonics in the grid current. Method-III uses a multi-resonant component-based grid-voltage full-weighed feedforward scheme [13], which introduces a series of quasi-resonant component $\boldsymbol{G}_{SR}$ into the grid voltage full feedforward path so that only the background harmonics in the grid voltage are fed forward as shown in Fig. 14(c), where the full-weighted feedforward function $\boldsymbol{G}_{ff}$ can be obtained through an equivalent transformation. Method-IV is the proposed impedance-decoupling-based reshaping method.

According to the control block diagrams of the four methods in Fig. 8 and Fig. 14, their complexities are also different. Method-I has the simplest structure, since no additional harmonic suppression branch is added beyond the baseline current control loop. Method-II and Method-III exhibit relatively high complexity, because multiple resonant branches are introduced at several harmonic frequencies in both the $\alpha$- and $\beta$-axes or in both the $d$- and $q$-axes. By comparison, the proposed method introduces resonant branches at selected frequencies in the $d$- and $q$-axes, enabling more targeted harmonic suppression. As a result, the number of resonant branches required by the proposed method is smaller than that in Method-II and Method-III.

Fig. 15 shows the measured waveforms of the PCC voltage and grid current under normal grid conditions. It is seen that without background harmonic disturbances in the grid

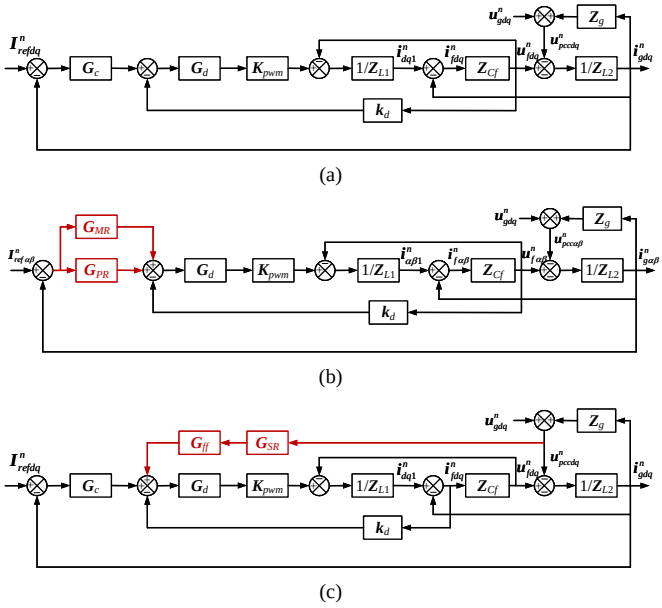


Fig. 14. Control block diagrams of the compared method. (a) Method-I. (b) Method-II. (c) Method-III.

TABLE II
DESCRIPTION OF THE FOUR COMPARED METHODS.

| Method | Technique |
|---|---|
| Method-I | Without harmonic suppression strategy |
| Method-II | Multiresonant controller [19], [20] |
| Method-III | Weighted grid voltage feedforward method [13] |
| Method-IV | Impedance-decoupling-based reshaping method |

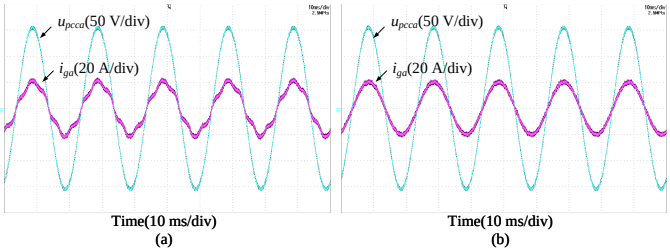


Fig. 15. Experimental waveforms of the PCC voltage and grid current under normal grid condition. (a) Method-I. (b) Method-IV.

voltage, distortions still exist in the grid current due to the low-frequency harmonics introduced by the NP voltage ripple as shown in Fig. 15(a). After applying the proposed impedance reshaping strategy, the distortions in the grid current are eliminated as shown in Fig. 15(b), which indicates that the proposed method can effectively suppress the harmonic disturbances introduced by NP voltage ripple.

To demonstrate the adaptability of the proposed method under weak-grid conditions, Fig. 16 presents the experimental waveforms with four methods in weak grids. The grid impedance is selected as 2.5 mH, corresponding to short-circuit ratio (SCR) of 10. With the relatively low grid impedance, all methods can ensure stable operation. As seen in Fig. 16(a) and Fig. 16(c), due to the lack of capability to suppress harmonic disturbance introduced by the NP voltage ripple, the grid currents of Method-I and Method-III exhibit distortions. Method-II provides resonance gain at harmonic frequencies, enabling suppression of low-frequency harmonics in the grid current as shown in Fig. 16(b). After adopting the proposed Method-IV, the harmonics in the grid current can also be effectively suppressed since the output impedance of $d$-axis is reshaped and the harmonics introduced by the NP voltage ripple flow into the inverter instead of the grid.

When the grid impedance is increased to 8 mH, corresponding to SCR of 3, the experimental waveforms of the four methods are shown in Fig. 17. Consistent with the experimental results in Fig. 16, Method-I and Method-III fail to eliminate distortions in the grid-connected current, whereas Method-II and Method-IV can effectively suppress them and maintain a nearly sinusoidal waveform. In addition, Method-I and Method-II provide no mitigation of the negative phase shift introduced by the PLL. Therefore, with the increase of grid impedance, the the system stability margin significantly decreases, leading to oscillations as shown in Fig. 17(a) and Fig. 17(b). In particular the introduction of the resonant controller further reduces the phase margin due to the resonant gain, exacerbating system oscillations.

To validate the effectiveness of the proposed method against multiple harmonic disturbance sources, Fig. 18 presents the experimental waveforms with four methods in the weak and seriously distorted grid with the grid impedance of 2.5 mH, where $7\%$ $5^{\text{th}}$, $5\%$ $7^{\text{th}}$, $3\%$ $11^{\text{th}}$ and $13^{\text{th}}$ harmonics are added to the grid. Without any suppression measures, the distortion of the grid current is further aggravated as shown in Fig. 18(a). After applying Method-III in 18(c), the distortion in the grid current is alleviated to some extent, but a large amount of low-frequency harmonics still remain. This is because the virtual impedance method based on PCC voltage feedforward can only suppress harmonic disturbance in the PCC voltage, while it is ineffective against the harmonic disturbance introduced by NP voltage ripple. The application of Method-II and Method-IV leads to a significant reduction of the distortion of the grid current as shown in Fig. 18(b) and Fig. 18(d). Nevertheless, with Method-II, the grid current still contains a small portion of low-frequency harmonics.

Fig. 19 presents the experimental waveforms with four strategies in seriously weak and distorted grid with the grid impedance of 8 mH. It is seen that the performance of the four methods in harmonic suppression is consistent with the experimental results in Fig. 18. However, with the weakening of grid strength, Method-I and Method-II become unstable, resulting in severe oscillations in the experimental waveforms. Therefore, among the four methods, only the proposed Method-IV is capable of ensuring stable operation under seriously weak and distorted grid conditions while simultaneously achieving wideband harmonic suppression.

To more clearly illustrate the harmonic suppression ability of the proposed method, Table III summaries the THD results of four methods under conditions of different grid impedance with distorted grids. As can be seen, the proposed Method-IV consistently achieves the lowest THD among all compared methods under both grid-impedance cases. When the grid impedance increases, the THD of Method-I and Method-II

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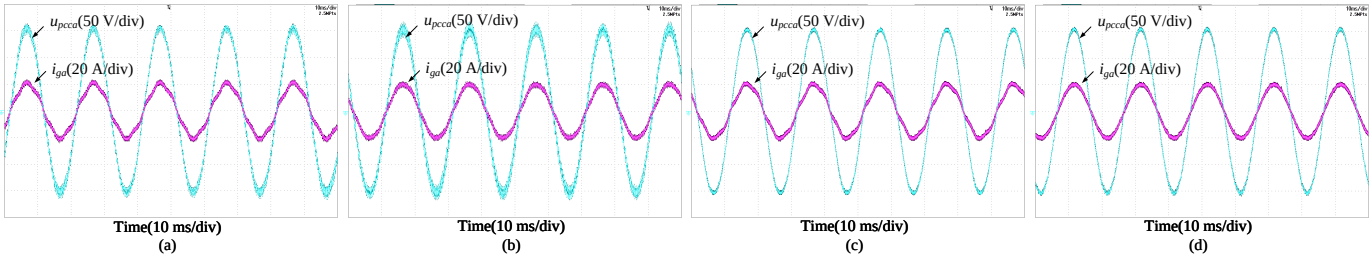


Fig. 16. Experimental waveforms of the PCC voltage and grid current under weak grid condition with $L_g$=2.5 mH. (a) Method-I. (b) Method-II. (c) Method-III. (d) Method-IV.

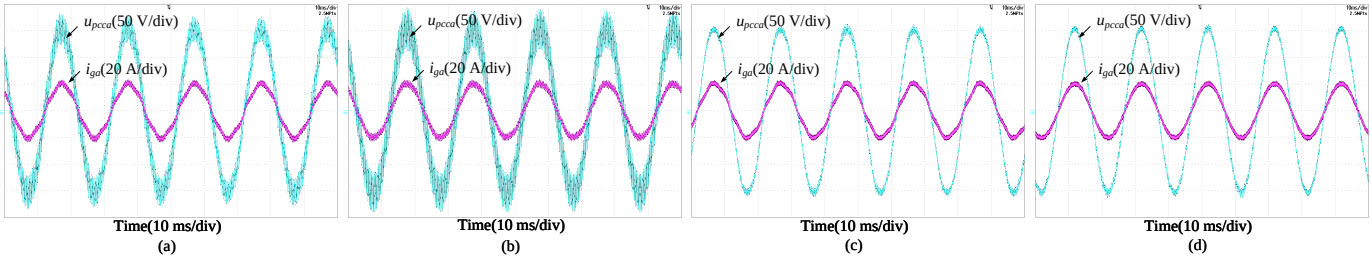


Fig. 17. Experimental waveforms of the PCC voltage and grid current under weak grid condition with $L_g$=8 mH. (a) Method-I. (b) Method-II. (c) Method-III. (d) Method-IV.

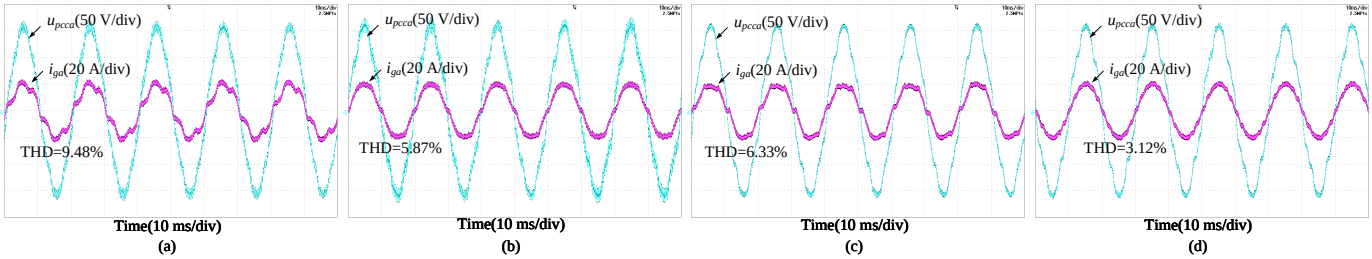


Fig. 18. Experimental waveforms of the PCC voltage and grid current under weak and seriously distorted grid condition with $L_g$=2.5 mH. (a) Method-I. (b) Method-II. (c) Method-III. (d) Method-IV.

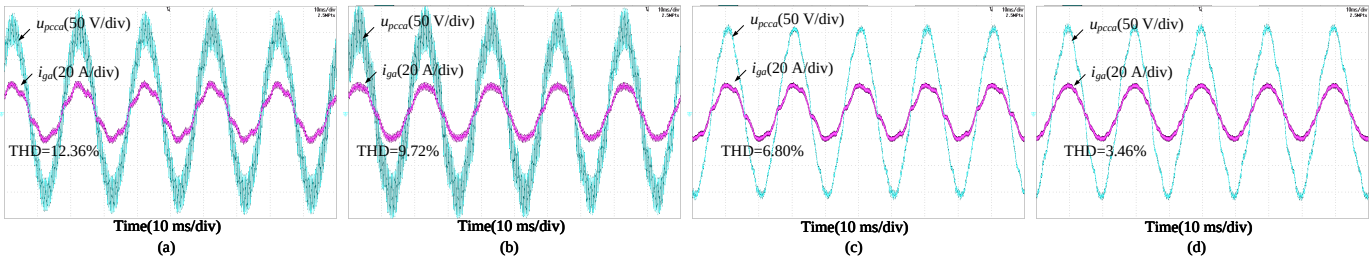


Fig. 19. Experimental waveforms of the PCC voltage and grid current under weak and seriously distorted grid condition with $L_g$=8 mH. (a) Method-I. (b) Method-II. (c) Method-III. (d) Method-IV.

rises noticeably, indicating degraded system stability. In contrast, the THD obtained by Method-III and Method-IV changes only slightly, demonstrating that both methods are highly robust against grid impedance variations. However, due to the limited harmonic suppression capability, the THD achieved by Method-III remains noticeably higher than that of Method-IV. Fig. 20 shows the grid current FFT diagrams of Method-III and the proposed Method-IV under distorted grid conditions with the grid impedance of 8 mH. It is seen from Fig. 20(a) that Method-III still exhibits a large presence of low-frequency harmonics, especially the $5^{\text{th}}$ and $7^{\text{th}}$ harmonics since it is powerless to suppress the harmonics introduced by NP voltage ripple. After adopting the proposed Method-IV, the $5^{\text{th}}$ and $7^{\text{th}}$ harmonics are significantly reduced, which indicates that

TABLE III
THE THD OF VARIOUS METHODS UNDER DIFFERENT CONDITIONS.

| Condition | Method-I | Method-II | Method-III | Method-IV |
|---|---|---|---|---|
| $L_g$=2.5 mH | 9.48% | 5.87% | 6.33% | 3.12% |
| $L_g$=8 mH | 12.36% | 9.72% | 6.80% | 3.46% |

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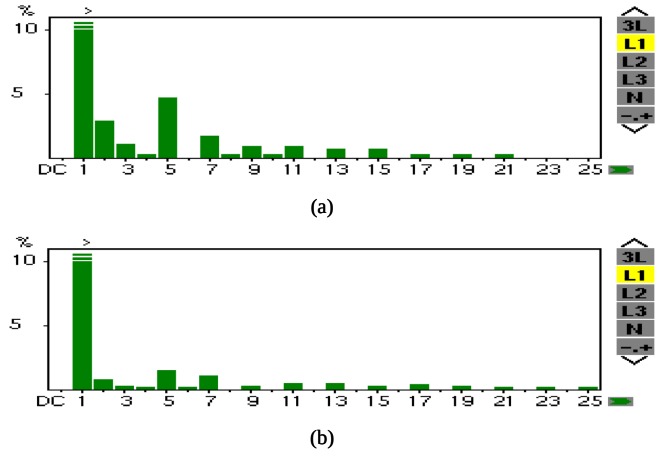


Fig. 20. Measured FFT diagrams of the grid current under weak and seriously distorted grid condition with $L_g$=8 mH. (a) Method-III. (b) Method-IV.

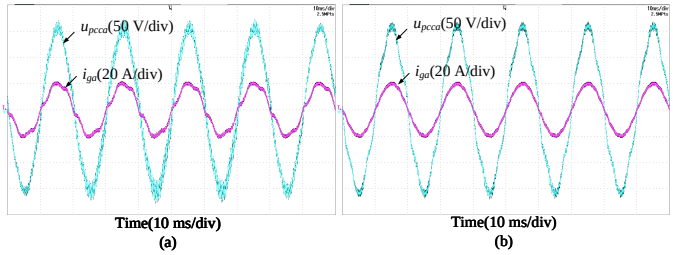


Fig. 21. Experimental waveforms under extremely weak and distorted grid conditions with $L_g$=15 mH. (a) Method-III. (b) Method-IV.

effective harmonic suppression is achieved across the entire low- and medium-frequency range.

To further validate the adaptability of the proposed method to extremely weak grid conditions, additional experiments with the grid impedance of 15 mH, corresponding to SCR of 1.5, are also carried out as shown in Fig. 21. It can be observed that under this extremely weak grid condition, Method-III becomes unstable, whereas the proposed Method-IV still remains stable, which demonstrates that the proposed impedance-decoupling-based reshaping method achieves the largest stability margin among the compared methods. In other words, the experimentally verified stable operating range of the proposed method is extended from SCR=3 down to SCR=1.5, whereas Method-III can no longer ensure stable operation at SCR=1.5. By contrast, according to Fig. 17 and Fig. 19, Method-I and Method-II becomes unstable at SCR=3. Therefore, among the compared methods, Method-I and Method-II exhibit the smallest stable operating range, Method-III can further extend the stability range to some extent, while the proposed Method-IV achieves the widest stable operating range. This further confirms the clear advantage of the proposed method in enhancing system stability under weak grid conditions.

In addition to the above steady-state tests, further experiments are carried out under non-ideal operating conditions to evaluate the robustness of the proposed method. Fig. 22(a) presents the results under a non-unity power factor condition, where reactive power is injected while keeping the active current reference unchanged. It can be observed

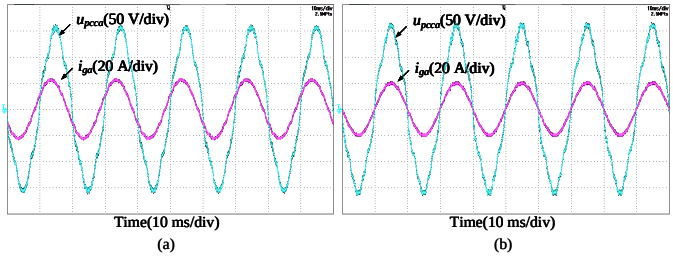


Fig. 22. Experimental waveforms of Method-IV under non-ideal operating conditions in a weak and seriously distorted grid with $L_g$=8 mH. (a) Reactive current injection with $I_{refq}$=10 A. (b) Injection of 3% $9^{\text{th}}$ and $15^{\text{th}}$ harmonic components.

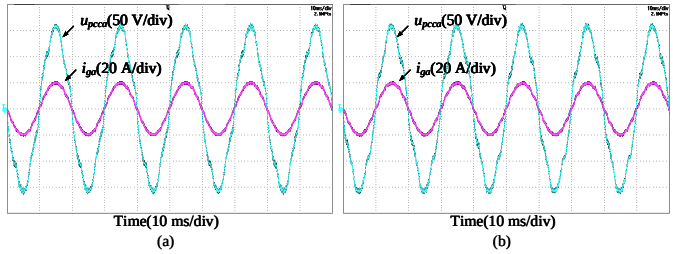


Fig. 23. Experimental waveforms of Method-IV under weak and seriously distorted grid conditions with $L_g$=8 mH and phase-shifted $5^{\text{th}}$ and $7^{\text{th}}$ background harmonics. (a) $-30°$ phase shift. (b) $+30°$ phase shift.

that the proposed method remains effective in maintaining a nearly sinusoidal grid current waveform and stable operation, indicating that the impedance decoupling based reshaping strategy is still applicable when reactive power is involved. Fig. 22(b) shows the experimental results when intermediate-order background harmonics (e.g., the $9^{\text{th}}$ and $15^{\text{th}}$) are additionally injected into the PCC voltage. The grid current distortion is still effectively suppressed, demonstrating that the proposed method can also mitigate intermediate-frequency harmonic disturbances beyond the low-order harmonics, and thus offers robust harmonic suppression performance under distorted grid conditions.

Fig. 23 presents the experimental results under weak and seriously distorted grid condition when the phase of the $5^{\text{th}}$ and $7^{\text{th}}$ harmonics is shifted by $\pm 30°$. It is seen that despite the phase variations of the $5^{\text{th}}$ and $7^{\text{th}}$ components in the background harmonics, the proposed method still achieves high suppression efficiency at the targeted harmonic frequencies, as the virtual impedance $Z_p$ and $Z_s$ maintain effective impedance shaping at these frequencies and thus suppress the corresponding grid current harmonics.

Fig. 24 presents the experimental results with the PLL bandwidth varied by +50%. As can be seen, when the PLL bandwidth is increased by 50%, which significantly reduces the stability margin and makes the system more prone to oscillations, the proposed method still maintains stable operation. The grid current remains well controlled, with the low- and medium-frequency harmonics effectively suppressed. Therefore, the proposed controller exhibits strong robustness against PLL bandwidth variation, maintaining stable operation even when the PLL bandwidth varies by ±50%.

Fig. 25 presents the experimental results under grid fre-

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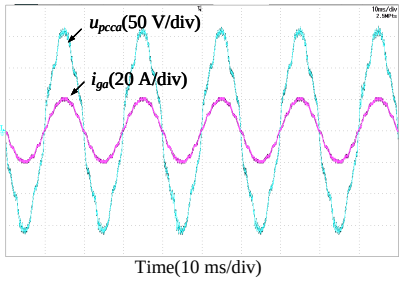


Fig. 24. Experimental waveforms of Method-IV under weak and seriously distorted grid condition with $L_g$=8 mH when the PLL bandwidth is increased by 50%.

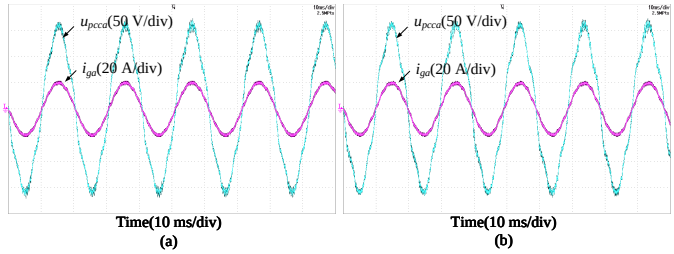


Fig. 25. Experimental waveforms of the proposed method under weak and distorted grid conditions with $L_g$=8 mH. (a) $f_0$=49.5 Hz. (b) $f_0$=50.5 Hz.

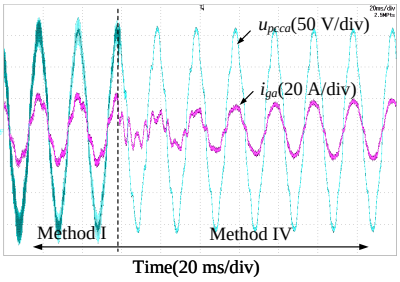


Fig. 26. Dynamic experimental waveforms under weak and seriously distorted grid condition with $L_g$=8 mH when changing from Method-I to Method-IV.

quency deviations of ±0.5 Hz. As can be observed, although the frequency offset shifts the actual locations of the targeted harmonic components, the proposed method still maintains the expected suppression performance and stable operation in both cases, since the designs of both $Z_p$ and $Z_s$ already take the allowable grid-frequency fluctuation range into account, rather than being centered on only one exact frequency. Therefore, the proposed method is not overly sensitive to grid frequency deviation, and its fundamental harmonic suppression and stability enhancement mechanism remains effective.

To verify the dynamic performance of the proposed method, Fig. 26 shows dynamic experimental waveforms with seriously weak and distorted grid when switching from Method-I to the proposed Method-IV, where the system stability is significantly improved and the grid current distortion is effectively eliminated. Fig. 27 presents the currents transient response. When the reference current steps from 10 A to 20 A, the system remains stable and the current is tracked quickly, which means that the bandwidth of the PLL is wide enough while ensuring system stability and harmonic suppression.

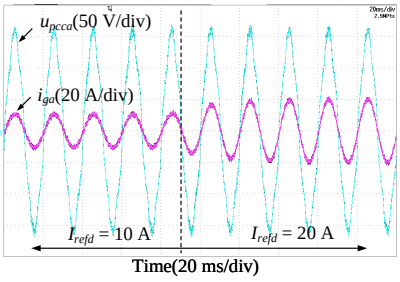


Fig. 27. Dynamic experimental waveforms of Method-IV under weak and seriously distorted grid condition with $L_g$=8 mH when the reference current is stepped from 10 A to 20 A.

Despite these advantages in harmonic suppression and stability improvement, a limitation of the proposed strategy is that different virtual impedances need to be designed for the $d$-axis and $q$-axis, which introduces additional computational burden compared with the conventional dual-loop current control with PI controller in the $dq$-frame, i.e., Method-I. The separate impedance designs in both axes require more arithmetic operations and state updates per sampling period in real-time control. Fortunately, with the continuous advancement of Digital Signal Processor (DSP) performance, this added computational burden is being gradually alleviated, making the proposed strategy practical without noticeably compromising performance.

## V. Conclusion

In this paper, an impedance reshaping method based on impedance decoupling in the $dq$-frame for mitigating the current harmonics from multiple harmonic disturbance sources is presented. By incorporating the effect of the PLL into the harmonic impedance model, it is revealed that the PLL reduces the q-axis impedance, which aggravates harmonics caused by background harmonic disturbances in the PCC voltage, while providing a low-impedance path for harmonics introduced by NP voltage ripple. To address this issue, parallel and series virtual impedances are designed in the $dq$-frame to reshape the internal and external impedance of the inverter. Compared with existing harmonic suppression methods, the proposed method incorporates the adverse impact of the PLL on harmonics and realizes harmonic suppression while maintaining stability under weak grid conditions. Experimental results comparing different harmonic suppression methods under weak and distorted grid conditions verify the effectiveness of the proposed method.

## References

[1] H. Liu, T. Fang, Y. Zhang, Z. Lin, and Y. Zhu, "Robust control method based on μ-synthesis theory and genetic algorithm for grid-connected inverter to cope with multiple uncertainties under weak grid," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 13, no. 1, pp. 615–625, 2025.

[2] O. Karimzada and G. De Donato, "Design and verification of a gan-based, single stage, grid-connected three-phase pv inverter," *IEEE Transactions on Power Electronics*, vol. 40, no. 4, pp. 5496–5504, 2025.

[3] Z. Hu, X. Xing, H. Zhang, and F. Blaabjerg, "Modeling and suppression method of low order harmonics for three-level inverter with small capacitance value," *IEEE Transactions on Industrial Electronics*, vol. 72, no. 1, pp. 470–480, 2025.

[4] J. Xu, J. Zhong, J. Kang, W. Dong, and S. Xie, "Stability analysis and robust parameter design of dc-voltage loop for three-phase grid-connected pv inverter under weak grid condition," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 4, pp. 3776–3787, 2024.

[5] K.-H. Kim, S. Cui, and J.-J. Jung, "Current-oriented phase-locked loop method for robust control of grid-connected converter in extremely weak grid," *IEEE Transactions on Power Electronics*, vol. 39, no. 10, pp. 11 963–11 968, 2024.

[6] X. Li, J. Fang, Y. Tang, X. Wu, and Y. Geng, "Capacitor-voltage feedforward with full delay compensation to improve weak grids adaptability of lcl-filtered grid-connected converters for distributed generation systems," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 749–764, 2018.

[7] T. Fang, H. Liu, H. Zhang, and C. Liu, "Robust technique using the optimized grid voltage feedforward to conquer the impact induced by dual factors for grid-connected inverter in weak grid," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 7, pp. 7199–7209, 2024.

[8] R. Raj Kar and R. Wandhare, "Passivity principle-based active damper design to enhance stability of a voltage source converter for weak grid scenario," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 5, pp. 5076–5089, 2024.

[9] J. Ye, H. Wang, B. Li, Y. Huang, J. Xu, and A. Shen, "Passivity-based controller design of pcc voltage feedforward active damping for grid-connected inverters," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 8, pp. 8752–8762, 2024.

[10] B. Chen, W. Wu, C. Gao, M. Orabi, E. Koutroulis, H. Chung, and F. Blaabjerg, "A new stability enhancement method using kf estimation for the pwm-smc-based grid-tied inverter under weak grid condition," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 6950–6959, 2022.

[11] M. E. Akdogan, D. Ramasubramanian, and S. Ahmed, "Control and stability analysis of grid-connected inverters in an unbalanced and distorted weak grid using mdsogi based selective virtual impedance," *IEEE Transactions on Industry Applications*, vol. 61, no. 2, pp. 2182–2192, 2025.

[12] S. Luo, W. Wu, E. Koutroulis, H. S.-H. Chung, and F. Blaabjerg, "A new kalman-filter-based harmonic current suppression method for the virtual oscillator controlled grid-tied inverter," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 12, no. 1, pp. 251–259, 2022.

[13] Z. Lin, X. Ruan, L. Wu, H. Zhang, and W. Li, "Multi resonant component-based grid-voltage-weighted feedforward scheme for grid-connected inverter to suppress the injected grid current harmonics under weak grid," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9784–9793, 2020.

[14] X. Chen, Y. Zhang, S. Wang, J. Chen, and C. Gong, "Impedance-phased dynamic control method for grid-connected inverters in a weak grid," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 274–283, 2017.

[15] C. Zhuo, X. Zhang, W. Song, and H. Yi, "Active resonant damper with control strategy based on inverter output conductance optimization under weak grid conditions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 3, pp. 2936–2946, 2024.

[16] K. Zhu, P. Sun, L. Zhou, X. Du, and Q. Luo, "Frequency-division virtual impedance shaping control method for grid-connected inverters in a weak and distorted grid," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 8116–8129, 2020.

[17] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A review of passive power filters for three-phase grid-connected voltage-source converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 1, pp. 54–69, 2016.

[18] G. Li, H. Wu, J. Chen, and X. Liu, "A harmonic current self-compensation control strategy of dc active power filter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 13, no. 4, pp. 5252–5261, 2025.

[19] M. Castilla, J. Miret, A. Camacho, J. Matas, and L. G. de Vicuna, "Reduction of current harmonic distortion in three-phase grid-connected photovoltaic inverters via resonant current control," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1464–1472, 2013.

[20] M. Castilla, J. Miret, J. Matas, L. Garcia de Vicuna, and J. M. Guerrero, "Control design guidelines for single-phase grid-connected photovoltaic inverters with damped resonant harmonic compensators," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4492–4501, 2009.

[21] G. Zhang, Q. Zhao, Y. Ye, A. Wang, S. Wen, and Y. Wang, "Feedforward repetitive control for grid-tied inverters in microgrids: Analysis, design, and verification," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 9, pp. 11 239–11 249, 2024.

[22] Q. Wang, Q. Zhao, and Y. Xia, "A novel voltage-sensorless grid voltage full feedforward estimator-based current control strategy for a grid-connected inverter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 72, no. 9, pp. 1233–1237, 2025.

[23] L. Huang and F. Blaabjerg, "A reference frame rematching method for enhancing large-signal stability of grid-following inverter under weak grid," *IEEE Transactions on Power Electronics*, vol. 40, no. 4, pp. 6135–6146, 2025.

[24] P. Alinaghi Hosseinabadi, H. Pota, S. Mekhilef, G. Konstantinou, M. Negnevitsky, and S. Mohamadian, "Three-phase phase-locked loop based on terminal sliding mode for grid-connected inverters," *IEEE Transactions on Industrial Electronics*, vol. 72, no. 5, pp. 4776–4787, 2025.

[25] X. Xiong and B. Luo, "Impedance reshaping method based on compensating pll dynamic to improve active power transfer capability of vsc under weak grid," *IEEE Transactions on Power Electronics*, vol. 40, no. 1, pp. 422–434, 2025.

[26] D. Zhu, S. Zhou, X. Zou, and Y. Kang, "Improved design of pll controller for lcl-type grid-connected converter in weak grid," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4715–4727, 2020.

[27] J. Yu, X. Lin, D. Song, R. Yu, Y. Li, and M. Su, "Harmonic instability and amplification for grid-connected inverter with voltage harmonics compensation considering phase-locked loop," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 3944–3959, 2020.

[28] G. Lou, Q. Yang, W. Gu, X. Quan, J. M. Guerrero, and S. Li, "Analysis and design of hybrid harmonic suppression scheme for vsg considering nonlinear loads and distorted grid," *IEEE Transactions on Energy Conversion*, vol. 36, no. 4, pp. 3096–3107, 2021.

[29] J. Fang, X. Li, H. Li, and Y. Tang, "Stability improvement for three-phase grid-connected converters through impedance reshaping in quadrature-axis," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8365–8375, 2018.

[30] B. Guo, X. Zhang, H. Ma, Y. Yang, X. Wang, Q. Tian, and S. Jin, "A series impedance reshaping control method considering pll dynamics for grid-connected inverters under weak grid conditions," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 5, pp. 4896–4910, 2024.

[31] "Ieee application guide for ieee std 1547™-2018, ieee standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces," *IEEE Std 1547.2-2023 (Revision of IEEE Std 1547.2-2008)*, pp. 1–291, 2024.

[32] F. Wang, J. L. Duarte, M. A. M. Hendrix, and P. F. Ribeiro, "Modeling and analysis of grid harmonic distortion impact of aggregated dg inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 786–797, 2011.